IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AF 2100

Applicant: Jeffrey S. Mailloux et al.

Title: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

#34

Docket No.: 303.623US4
Filed: December 3, 1997
Examiner: Hong Kim
Customer No.: 21186

Serial No.: 08/984563
Due Date: November 12, 2003
Group Art Unit: 2186
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(GENERAL)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Jeffrey S. Mailloux et al.	)	Examiner: Hong C. Kim
	)	
Serial No.: 08/984,563	)	Group Art Unit: 2186
	)	
Filed: December 3, 1997	)	Docket: 303.623US4
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For: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION	)	

APPELLANTS' SUPPLEMENTAL BRIEF ON APPEAL

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Appeal Brief is presented to request reinstatement of the Appeal initiated with the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on March 14, 2003, and as a response to the Final Rejection of claims 36-39, 59-69, and 75-83 of the above-identified application, as set forth in the Final Office Action mailed on August 12, 2003.

This Appeal Brief is filed in triplicate. The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims 36-39, 59-69, and 75-83.

APPELLANTS' SUPPLEMENTAL BRIEF ON APPEAL

TABLE OF CONTENTS

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the Assignee, Micron Technology, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There are four other appeals known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. The related appeals that are currently pending before the Board concern U.S. Patent Application Serial Numbers 08/984,560; 08/984,562; and 08/984,701. The fourth appeal was filed in U.S. Patent Application Serial Numbers 08/984,561. U.S. Patent Application Serial Numbers 08/984,561 was allowed by the examiner after the original Appeal Brief was filed.

3. STATUS OF THE CLAIMS

Claims 36-39, 59-69, and 75-83 are currently pending and appealed. No claims have been canceled or added. The pending claims are listed in Appendix I.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action mailed January 14, 2003.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, the embodiments disclosed relate to a memory device that selectably operates using both burst and pipelined modes of operation. In one embodiment, a storage device 100 (shown in FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode

and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Pg. 29, lines 5-25). Some embodiments can switch between burst access and ... pipelined modes of operation without ceasing ("on the fly"). (Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is first used to select data within the device 100. A counter 149 included in the circuitry 122 then increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses external addresses 115 to access data within the device 100. (Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Pg. 8, lines 1-5). In addition to the embodiments described herein, other embodiments of varying scope, including systems, methods, and storage devices, such as memory circuits, are disclosed. (Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

Whether claims 36-39, 59-64, 69, and 75-83 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning, hereinafter "Manning".

7. GROUPING OF CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal.

8. ARGUMENT

a) The Applicable Law

Establishing anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires

the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

b) The Reference

Manning: teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture to Manning's invention is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of how to apply the architecture, or its operation, are given.

c) Discussion of the Rejection under § 102

Claims 36-39, 59-64, 68-69, and 75-83 were rejected under 35 USC § 102(e) as being anticipated by Manning. First, the Appellants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because Manning does not disclose each and every element of claims 36-39, 59-64, 68-69, and 75-83. Therefore, the Appellants respectfully traverse this rejection under 35 U.S.C. § 102(e).

c.1. Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning specifically fails to disclose "selecting between a burst mode and a pipelined mode of operation" as claimed by the Appellants in claim 36 or selecting a burst mode of operation or a pipeline mode of operation as claimed by Appellants in claims 63 and 68. Similarly, Manning fails to disclose the order of address access "in the pipelined mode" (claims 37, 76, and 81), or "in the burst mode" in conjunction with selecting between the burst and pipelined modes of operation (claim 38); or "selecting at least one address pathway based on the selection between the burst mode and the pipelined mode" (claim 39).

Further, Manning fails to teach "choosing whether the memory is in a burst mode ... or in a pipeline mode of operation", "switching between the burst mode ... and the pipelined mode", "switching between ... read ... and write operation[s]" in conjunction with choosing a pipelined mode of operation, or "operations ... performed in a different order" in conjunction with choosing a pipelined mode of operation (claims 59-62).

In addition, Manning fails to describe "selecting an external address only data path ... if ... the pipelined mode of operation is selected" (claim 63), or "operations ... performed in a different order" (including selecting a pipelined mode of operation) (claim 64). Manning also fails to describe "changing [a] ... mode select signal to select a pipelined mode of operation" (claims 65 and 67), and "switching the mode of operation to a pipelined mode" (claim 66). Manning further fails to disclose "selecting an external address only data path, obtaining an external column address, and accessing the memory when the pipeline mode of operation is selected" (claim 68).

Finally, Manning fails to include any teaching of "switching from a burst mode ... to a pipelined mode" (claims 75 and 80), "selecting at least one address pathway" based upon such switching (claims 77 and 82), "subsequently switching from the pipelined mode ... to the burst mode" (claims 78 and 83), or "selecting at least one address pathway" based upon such subsequent switching (claim 79). Manning also fails to describe a storage device including mode circuitry "configured to select between a burst mode and a pipeline mode" along with "an external column address data path for pipeline read and write operation column address generation" (claim 69).

Several assertions were made in the Office Action which attribute support to various concepts allegedly disclosed by Manning. However, a careful reading of each citation reveals errors with respect to the asserted elements. These assertions have been made with respect to:

Claim 36, 59, 60, 75, and 80 - Manning does not disclose switching, selecting, or choosing between a burst mode and a pipelined mode (Manning never discusses switching or selecting between the modes, only operation in the burst mode, and the possibility of using a pipelined architecture).

Claims 36, 59, 63, 68, 75, and 80 - Manning does not teach that "one has to select a pipelined mode if one is in a burst mode (burst mode operations and a pipelined mode of operation are completely independent of each other, as noted below).

Claims 37, 76, and 81 - Manning does not disclose obtaining a second external column address ... for operation in the pipeline mode (Manning merely refers to the possibility of using a pipelined *architecture*, and never discusses the details of how it might operate).

Claim 39, 77, 82 - Manning does not disclose selecting an address pathway based on ... selection between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 63 and 69 - Manning does not disclose an external address only path for the pipeline mode, or pipeline/burst circuitry (since Manning explains nothing about a pipelined architecture, other than generally characterizing its operation).

Claims 63, 68, 69, and 79 - Manning does not teach "... during the pipelined mode, an external counter/latch path is selected." (since Manning explains nothing about a pipelined architecture, other than generally characterizing its operation).

Claims 78, 79, and 83 - Manning does not disclose, discuss, or teach switching from pipelined mode to burst mode (Manning merely refers to the possibility of using a pipelined *architecture*).

c.2. Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline

mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and pipelined modes of operation, as claimed in claims 36, 59, 63, 65, 66, 67, 68, 69, 75, and 80 (and in all claims that depend from them)?

Second, the Office has failed to establish a case of anticipation. While the assertion is made that Manning discloses "choosing whether the memory is in burst or a pipelined mode of operation","switching between a burst mode and a pipeline mode", and "pipeline/burst circuitry", the Appellants' representative, after a careful study of Manning, was unable to locate any such discussion, nor any such circuitry which was configurable to select or switch between burst and pipelined modes of operation.

For example, the only elements offered by the Office to support the assertion that Manning "discloses the invention as claimed" with respect to claims 36, 75, and 80 are: FIG.1 Refs. 26, 38, 40, and EDO signal, and FIG. 2 ADDR, ROW, COLm, and /WE signals; col. 5, lines 43-50; col. 6, lines 14-34; and col 7, lines 43-54. Fig. 1 is a block diagram of an EDO memory that operates in burst or page modes, with no indication regarding exactly which modes may be operative, or how they may be selected. Reference labels 26, 38, and 40 refer to a counter, a control circuit, and a mode register, respectively. The mode register 40 is never discussed in conjunction with pipelined mode operations - only burst, fast page, and static column modes. Col. 5, lines 41-50 discuss the possibility of using a pipelined architecture, but not as enabling switching between pipeline mode and burst operations within the *same* memory, as disclosed and claimed by the Appellants. Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, or circuitry to effect such a selection, as claimed by the Appellants in independent claims 36, 59, 63, 65, 66, 67, 68, 69, 75, and 80, and all of the claims which depend from them.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of *internal* addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for "Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as Appendix II.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.

Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See "Fast Page Mode (FPM)", Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See "Extended Data Output RAM (EDO)", Id.

Burst EDO memory improves EDO performance by adding **a pipeline stage** (i.e., **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the

initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined by the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id.

As a matter of contrast, in some embodiments of the Appellants' invention, a newburst signal from control logic is provided. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with a stored initial external address. A counter is then used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through the memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held active, and /CAS is cycled, a random or determined order of columns associated with the row address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of columns may be accessed. (Application, Pg. 8, lines 1-13)

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection under § 102 is improper. Reconsideration and allowance of claims 36-39, 59-64, 69, and 75-83 is respectfully requested.

c.3 Why the claims are separately patentable.

While the separate patentability of each claim has been discussed in the "argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 36 includes "selecting between a burst mode and a pipelined mode of operation of ... [an] asynchronously accessible DRAM". Dependent claims 37-39 refine this concept by including the limitations on the order of address access "in the pipelined mode" (claims 37), or "in the burst mode" in conjunction with selecting between the burst and pipelined modes of operation (claim 38); and "selecting at least one address pathway based on the selection between the burst mode and the pipelined mode" (claim 39). Manning does not disclose these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from independent claim 36.

Independent claim 59 includes the element of "choosing whether the memory is in a burst mode ... or in a pipeline mode of operation". Dependent claims 60-62 add the limitations of "switching between the burst mode ... and the pipelined mode", "switching between ... read ... and write operation[s]" in conjunction with choosing a pipelined mode of operation, and "operations ... performed in a different order" in conjunction with choosing a pipelined mode of operation. Manning does not disclose these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from independent claim 59.

Independent claim 63 includes "selecting an external address only data path ... if ... the pipelined mode of operation is selected" and "receiving an external row address". Dependent claim 64 adds the further limitation of "operations ... performed in a different order" (including selecting a pipelined mode of operation). Manning does not disclose these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, as well as from the independent claims.

Independent claim 65 and 67 include "changing [a] ... mode select signal to select a pipelined mode of operation", while dependent claim 66 adds the limitation of "switching the mode of operation to a pipelined mode". Independent claim 65 includes the additional limitation of "receiving a mode select signal". Manning does not disclose these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other.

Independent claim 68 includes "selecting an external address only data path ... when the pipelined mode of operation is selected." Manning does not disclose these elements. This independent apparatus claim is separately patentable from all of the other claims.

Independent claim 69 describes a storage device including mode circuitry "configured to select between a burst mode and a pipeline mode" along with "an external column address data path for pipeline read and write operation column address retrieval". Manning does not disclose these elements. This independent apparatus claim is separately patentable from all of the other claims.

Independent method claims 75 and 80 include the element of "switching from a burst mode ... to a pipelined mode", while dependent claims 77 and 82 add the limitation of "selecting at least one address pathway" based upon such switching. Dependent claims 78 and 83 add the limitation of "subsequently switching from the pipelined mode ... to the burst mode". Dependent claim 79 adds the limitation of "selecting at least one address pathway" based upon such subsequent switching. Independent claim 75 adds the possiblity of "selecting a ... write operation." Manning does not disclose these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, as well as from the independent claims.

c.4 Response by Appellants to general arguments in the Final Office Action.

First, it is asserted in the Office Action that "accessing a non burst ... standard EDO memory ... is accomplished by overlapping memory operations using a pipe" and that "one has to select a pipelined mode if one is in a burst mode." However, there is no support whatever for such statements in Manning.

Several other statements of alleged fact, unsupported by any reference, are presented in the Final Office Action. While the Appellants have repeatedly requested evidentiary support for similar statements, none has been given. A few of these statements are quoted below:

"it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input, or memory data output to be processed simultaneously";

"the pipelined architecture requires only a single sample-and-hold circuit per read or write circuit"; and

"the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area."

However, other than these unsupported statements, there is no evidence whatsoever that Manning teaches this specific type of operation or construction. The text of Col. 7, lines 50-54 merely states "A more complex memory device may provide additional modes ... such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time." There is simply no description of a pipelined mode of operation in Manning, let alone switching between a pipelined mode and another mode. Further, as explained in the original Appeal Brief (see Appeal Brief pgs. 11-12), and in the reference attached hereto as Appendix II, none of these modes necessarily have anything to do with a true pipelined mode of operation. Thus, the assertion that Manning teaches a pipelined mode of operation is simply not supported by the evidence in the record.

Since there is no evidence in the record to support the Examiner's assertion, the Examiner appears to be using personal knowledge. The Examiner is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) and M.P.E.P. § 2144.03.

Second, the many statements in the Office Action, including those made in the "Response to Amendment" section that " Manning (864) discloses selecting or switching between a burst mode and a pipelined mode" and "... switching between burst EDO mode and standard EDO mode" do not distinguish between the operation of a pipeline architecture (which may include a pipeline stage) and a pipeline mode, as described in detail by the Appellants (see Appeal Brief, pgs. 11-12). Nor do such statements take into account the following points made by the Appellants:

(a) Manning plainly does not disclose selecting or switching between pipelined and burst modes;

(b) the Office has admitted that "Manning [864] does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of

operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter; and

(c) the statement"... one has to select a pipelined mode if one is in a burst mode" mischaracterizes the operation of an EDO memory (e.g., an EDO memory with internal addresses generated using a pipeline stage/architecture does not require selecting a "pipelined mode" for operation by receiving *external addresses*, as defined by the Appellants). Further, as noted previously, there is no evidence in the record of this specific type of construction or operation in Manning.

Finally, it is respectfully noted that a Notice of Allowability (the "Notice") indicating allowance of all claims in a related matter, U.S. Patent Application Serial Number 08/984,561 (Attorney Reference: 303.623US6), has been received by the Appellants (Paper 32). The Office has admitted the deficiencies of Manning (864) therein with respect to several of the same elements which distinguish the claims of the instant Application. The attention of the Board is directed to the following assertions by the Appellants in the previously pending appeal of this related matter:

> "Manning Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning Col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, **Manning never discusses the ability to select or switch between burst and pipelined modes of operation**..." (emphasis added)

This language was approved by the Office in the Notice, which states: "The claims are allowable over the prior art of record [U.S. Patent No. 5,587,964, issued to Rosich et al. in view of Manning (864)] because the claims are distinguished from the prior art of record for the reasons as set forth in the ... appeal filed on 12/27/02 and because an update of a search previously made does not detect the combined claimed elements as set forth." For example, claim 72 in this related matter reads:

A method for switching between pipeline and burst modes of operation, comprising:

maintaining a first enabling signal in an active state, the first enabling signal being an address-strobe signal;

maintaining an external mode select signal to select a pipeline mode;

receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

switching the mode of operation to a burst mode on successive cycles of the second enabling signal while maintaining the first enabling signal in the active state.

Thus, the Office agrees that Manning (864) does not teach the ability to select or switch between burst and pipelined modes of operation, and the standard of § 102 has not been met, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

c.5 Double patenting rejection.

Claims 65-67 were provisionally rejected under the judicially created doctrine of double patenting over claims 51, 59, 63, 64, and 67 of related and co-pending Application Serial No. 08/984,561, presently allowed. The Appellants will file a Terminal Disclaimer to remove the double patenting rejection upon receipt of an indication that the claims in the instant Application are otherwise allowable.

9. SUMMARY

It is respectfully submitted that a *prima facie* case of anticipation under 35 U.S.C. §102 has not been established. Reconsideration and withdrawal of the rejection of claims 36-39, 59-64, 68-69, and 75-83 is therefore respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also requested.

The Examiner is invited to telephone the Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

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Date 14 Oct 2003 By _____

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Tina Kohat
Name

Signature

APPENDIX I

The Claims on Appeal

36. A method for accessing an asynchronously-accessible dynamic random access memory, comprising:

receiving an external row address to the asynchronously-accessible dynamic random access memory;

selecting between a burst mode and a pipelined mode of operation of the asynchronously-accessible dynamic random access memory;

selecting between a read operation and a write operation of the asynchronously-accessible dynamic random access memory; and

obtaining a first external column address for accessing the asynchronously-accessible dynamic random access memory.

37. The method, as in Claim 36, further comprising:

obtaining a second external column address subsequent to the first external column address for operation in the pipelined mode.

38. The method, as in Claim 36, further comprising:

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

39. The method, as in Claim 36, further comprising:

selecting at least one address pathway based on the selection between the burst mode and the pipelined mode.

59. A method of accessing a memory, comprising:

receiving an external row address;

choosing whether the memory is in a burst mode of operation or in a pipeline mode of operation;

selecting a read operation or a write operation for the memory; and

executing a read or write operation in the chosen mode of operation.

60. The method of claim 59, and further comprising:

switching between the burst mode of operation and the pipelined mode of operation.

61. The method of claim 59, and further comprising:

switching between the read operation and the write operation.

62. The method of claim 59, wherein the operations are performed in a different order.

63. A method of accessing a memory, comprising:

receiving an external row address;

selecting a burst mode of operation or a pipeline mode of operation of the memory;

selecting a read operation or a write operation for the memory;

selecting an external address only data path, obtaining an external column address, and obtaining information from the memory if the read operation of the pipeline mode of operation is selected;

selecting an external address only data path, obtaining an external column address, and providing information to the memory if the write operation of the pipeline mode of operation is selected;

selecting an initial buffered external address data path, obtaining an initial external column address, obtaining information from the memory, and generating internal column addresses and obtaining further information from the memory until all desired internal column addresses are used if the read operation of the burst mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an initial external column address, providing information to the memory, and generating internal column addresses

and providing further information to the memory until all desired internal column addresses are used if the write operation of the burst mode of operation is selected.

64. The method of claim 63, wherein the operations are performed in a different order.

65. A method of operating a memory circuit, comprising:

receiving a mode select signal;

receiving an initial external address;

selecting a read or a write operation of the memory;

cycling a second enabling signal multiply between active and inactive;

generating an internal address on a cycle of the second enabling signal based on the initial external address;

changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state; and

receiving an external address on each cycle of the second enabling signal.

66. A method for accessing a memory, comprising:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a burst mode of operation;

receiving an initial external address;

selecting a read or a write operation of the memory;

cycling a second enabling signal multiply between inactive and active;

generating an internal address on a cycle of the second enabling signal based on the initial external address; and

switching the mode of operation to a pipeline mode on successive cycles of the second enabling signal by changing the mode select signal.

67. A method for operating a memory, comprising:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a burst mode of operation;

selecting a read operation or a write operation of the memory;

receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

changing the mode select signal to select a pipeline mode of operation.

68. A method for data transfer direction selection in a memory, comprising:

selecting a read or a write operation of the memory;

selecting a burst or a pipeline mode of operation for the memory;

selecting an external address only data path, obtaining an external column address, and accessing the memory when the pipeline mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an inital external column address, accessing the memory, and generating internal column addresses when the burst mode of operation is selected.

69. A storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode;

selection circuitry for selecting between a read operation and a write operation;

an external column address data path for pipeline read and write operation column address retrieval;

an internal column address generation module for burst read and write operation column address generation; and

pipelined/burst circuitry coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the storage device in either mode.

75. A method for accessing an asynchronously-accessible dynamic random access memory (DRAM), comprising:

receiving an external row address to the asynchronously-accessible DRAM;

switching from a burst mode of operation to a pipelined mode of operation;

selecting a memory operation selected from a group consisting of a read operation and a write operation; and

obtaining a first external column address for accessing the asynchronously-accessible DRAM.

76. The method of claim 75, further comprising:

obtaining a second external column address subsequent to obtaining the first external column address for operation in the pipelined mode.

77. The method of claim 75, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.

78. The method of claim 75, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation;

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

79. The method of claim 78, further comprising:

selecting at least one address pathway based on subsequently switching to the burst mode of operation.

80. A method for accessing an asynchronously-accessible dynamic random access memory (DRAM), comprising:

receiving an external row address to the asynchronously-accessible DRAM;

switching from a burst mode of operation to a pipelined mode of operation;

selecting a memory read operation; and

obtaining a first external column address for accessing the asynchronously-accessible DRAM.

81. The method of claim 80, further comprising:

obtaining a second external column address subsequent to obtaining the first external column address for operation in the pipelined mode.

82. The method of claim 80, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.

83. The method of claim 80, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation; and

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

APPENDIX II

Reference

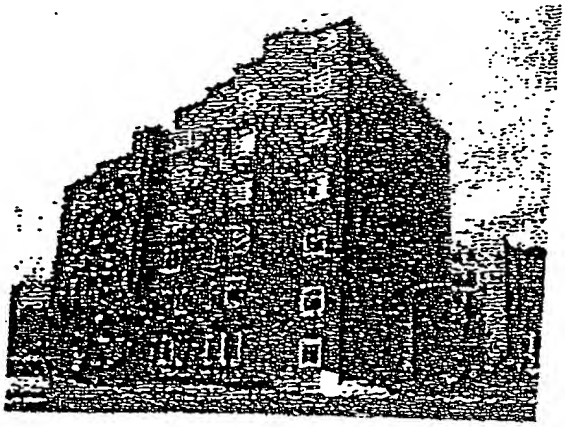
I. Other References

"Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999

Company

Shuttle

Home Company News Products Support Awards Certificates Comments Employment Where to buy



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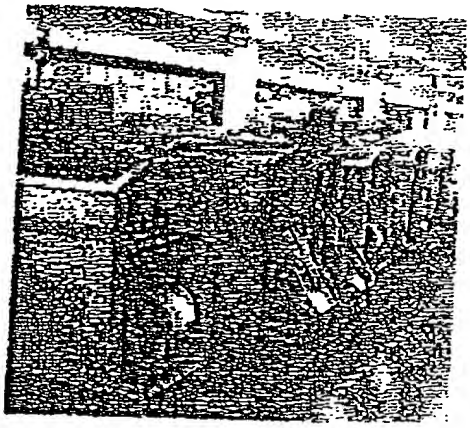
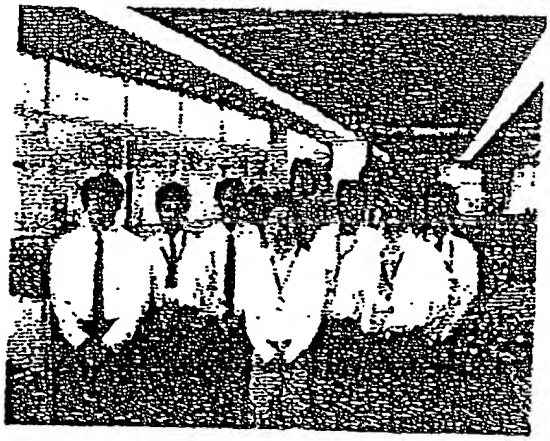
In order to ensure round-the-clock service & support, SHUTTLE is accessible by E-mail, Web site and BBS.





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The Research and Development engineers highly experienced and creative. For 1 professionals are always in pursuit of i maintaining product's price per performance quality. Fully equipped with hi-end CAD too intensive research of up-to-date technology, professionals at SHUTTLE have provided super have been proven in the market for over a dec

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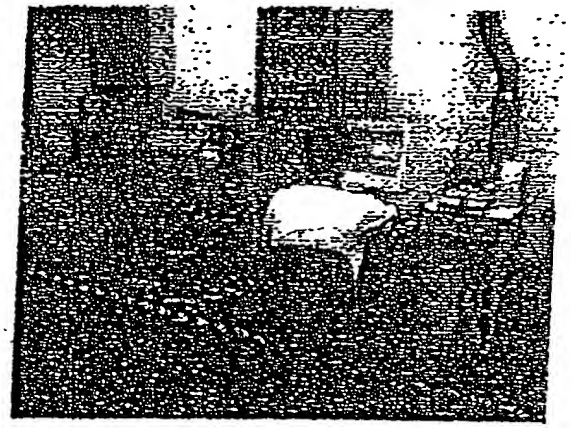
SHUTTLE is dedicated to TQM (Total Quality Management) principles. Only genuine brand name components are used in the products and strict QA/QC procedures are followed in the

manufacturing process. The manufacturing facilities feature the latest in SMT equipment and manufacturing technology. ISO9001, ISO9002, and ISO14000 certified, SHUTTLE's factories yield the total production capacity of over 300K units per month. In order to keeping pace with its rapidly expanding global markets, SHUTTLE is in the process of increasing its manufacturing capacity as additional SMT lines are implemented.



Environmental Policy

Our company is a member of the global together with the whole global enterprises t the green environment. We are dedicated protection of the environment and the environmental pollution, for the minimizing of handling of energy conservation, as well as to related legal requirements. This is to allow th be able to have our manufactured green p eventually protect our environment.

Our commitments:

- Strictly implement the laws and regulations
- Continuously improve the measures for preventing pollution
- Re-use the recyclable resources
- Conserve energy which shall be done by everyone
- Aspire for green products

Commitment to Customers

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SIMMs and DIMMs

Chapter set below:
SIMMs (Single In Line Memory Modules)
DIMMs (Dual In Line Memory Modules)

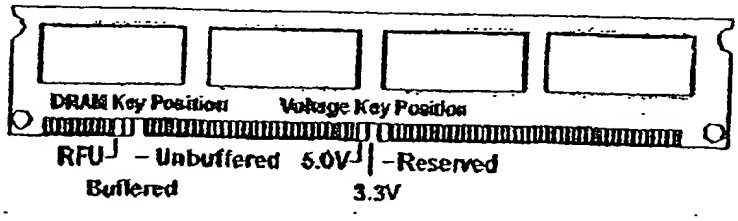
The names SIMM and DIMM only specifies the package RAM comes in, not the type! You can get each RAM type (FPM, EDO, SDRAM,...) for each module, but as fas as PCs are concerned, DIMMs are at present only used for SDRAM.

SIMMs (Single In Line Memory Modules)

SIMMs have 72 Pins and data path width of 32 Bit (36 Bit using Parity-Modules). On Pentium-Mainboards two SIMMs of the same kind and capacity have to be used to fill a bank. Some chipsets (for exp. SIS) allow to use only one module which results in a high performance loss.

DIMMs (Dual In Line Memory Modules)

DIMMs have 168 Pins. The data path width is 64 Bit (72 Bit using Parity-Modules). For this reason you can use a single DIMM to fill a bank on a Pentium-Board. Modules must be 3.3V Unbuffered SDRAM or EDO (you can identify type as shown by the illustration above).



Types of memory (FPM, EDO, SDRAM, ...)

Chapter set below:
Fast Page Mode (FPM)
Extended Data Output RAM (EDO)
Burst Extended Data Output RAM (BEDO)
Synchronous Dynamic RAM (SDRAM)

Fast Page Mode (FPM)

Fast Page Mode are standard memory modules. Actually VRAM or Video RAM is nothing much different, it only is so called dual ported, which means it can be accessed by the

RAMDAC independently of the CPU accesses via the second port, so that the RAMDAC doesn't have to wait for the CPU access to finish. FPM DRAMs for mainboards comes in two different flavors nowadays: 60ns and 70ns access time. On 66 MHz system-clock you should use 60ns modules, however, 70ns work in most cases as well. "Fast Page Mode" means that the module assumes that the next access is in the same memory area (ROW) to speed up the operation. The fastest access in CPU-Cycles is 5-3-3-3 for a data burst of 4 (Byte / Word / Dword).

Extended Data Output RAM (EDO)

The major difference between FPM and EDO is the timing of the CAS#-Signal and Data output using a latch. This speeds up sequential read-operations. The fastest access in CPU-Cycles is 5-2-2-2.

Burst Extended Data Output RAM (BEDO)

In opposition to EDO data latch on BEDO is replaced by a register (i.e. an additional latch stage is added) data will not reach the outputs as a result of the first CAS cycle. The benefit of this internal pipeline stage is that data will appear in a shorter time from the activating CAS edge in the second cycle (i.e. tcas is shorter). The second difference is that BEDO devices include an internal address counter so that only the initial address in a burst of four needs to be provided externally. The fastest access in CPU-Cycles is 5-1-1-1.

Synchronous Dynamic RAM (SDRAM)

As the name says already, this RAM is able to handle all input and output signals synchronized to the system clock - that is something a short while ago only Static Cache RAM was able to achieve. System clock can be higher than 66Mhz. „PC/100"-modules support 100 MHz clock frequency for chipsets with this feature (e.g. Intel 440BX or VIA MVP3). The fastest access in CPU-Cycles is 5-1-1-1 (as fast as BEDO).

Back to Top